# LAB 1: Prep sheet

* **Pls. upload to EMIL before the lab session by everyone and in PDF format only (otherwise no grading) and in addition**
* **give a hardcopy to the Prof/Lab Assistant at the beginning of the lab session**

**PREP TASK 1.1:** Derive the Boolean equations for the combinational logic of the tank controller (digital system with 4 inputs, 2 outputs).

Give the truth table for both output signals P1 and P2.

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| Boolean equations:    Truth table:   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | U | L | S1 | S2 | P1 | P2 | | 0 | 0 | 0 | 0 | 1 | 0 | | 0 | 0 | 0 | 1 | 1 | 0 | | 0 | 0 | 1 | 0 | 1 | 0 | | 0 | 0 | 1 | 1 | 1 | 0 | | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | 1 | 0 | 1 | 0 | 0 | | 0 | 1 | 1 | 0 | 1 | 1 | | 0 | 1 | 1 | 1 | 1 | 0 | | 1 | 0 | 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 1 | 0 | 1 | | 1 | 0 | 1 | 0 | 0 | 1 | | 1 | 0 | 1 | 1 | 0 | 1 | | 1 | 1 | 0 | 0 | 0 | 1 | | 1 | 1 | 0 | 1 | 0 | 1 | | 1 | 1 | 1 | 0 | 0 | 1 | | 1 | 1 | 1 | 1 | 0 | 1 | |

**PREP TASK 1.2**: Convert the Boolean expressions from PREP TASK 1.1 into a NAND2 representation and draw the schematic of a realization with two SSI-devices 7400 which comprise four NAND2 gates each.

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| Implementation of the Boolean equation for P1:    Schematic:      74HC00 74HC00 |

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| Implementation of the Boolean equation for P2:    Schematic:      74HC00 74HC00 |

**PREP TASK 3.1:** Give the output Vout when the switch at the input of the first NAND2 gate is in position GND (input connected to low). Label all relevant signals with its value (LOW/HIGH) in the schematic.

Explain: What happens when the switch is in position Vcc?

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| Signal values when switch connected to GND:   |  |  |  |  | | --- | --- | --- | --- | | A | B | A AND B | A NAND B | | L | L | L | H | | L | H | L | H | | H | L | L | H | | H | H | H | L |   Output when switch connected to Vcc:  Since Vcc produces H, then for the first time we will try adding L input for gate 1.    For the second time we will try adding H input for gate 1.    Again, we see a contradiction. Thus, if we turn the switch to Vcc, then it won’t work as normally as in case when the switch is turned to GND. |

**PREP TASK 4.1:** Draw the signals D1, Q1 and Q2 for 5 periods of the clock signal. Assume the start condition is Q1=Q2=LOW (i.e. condition after reset).

Draw the schematic using a 74HC175 Quad D-type flip-flop and a 74HC7266 Quad 2-input XNOR device.

HINT: Download the datasheets from the internet if you need further details on the pin assignment of the devices.

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| Timing diagram for D1, Q1, Q2    Schematic |